

FIG. 1

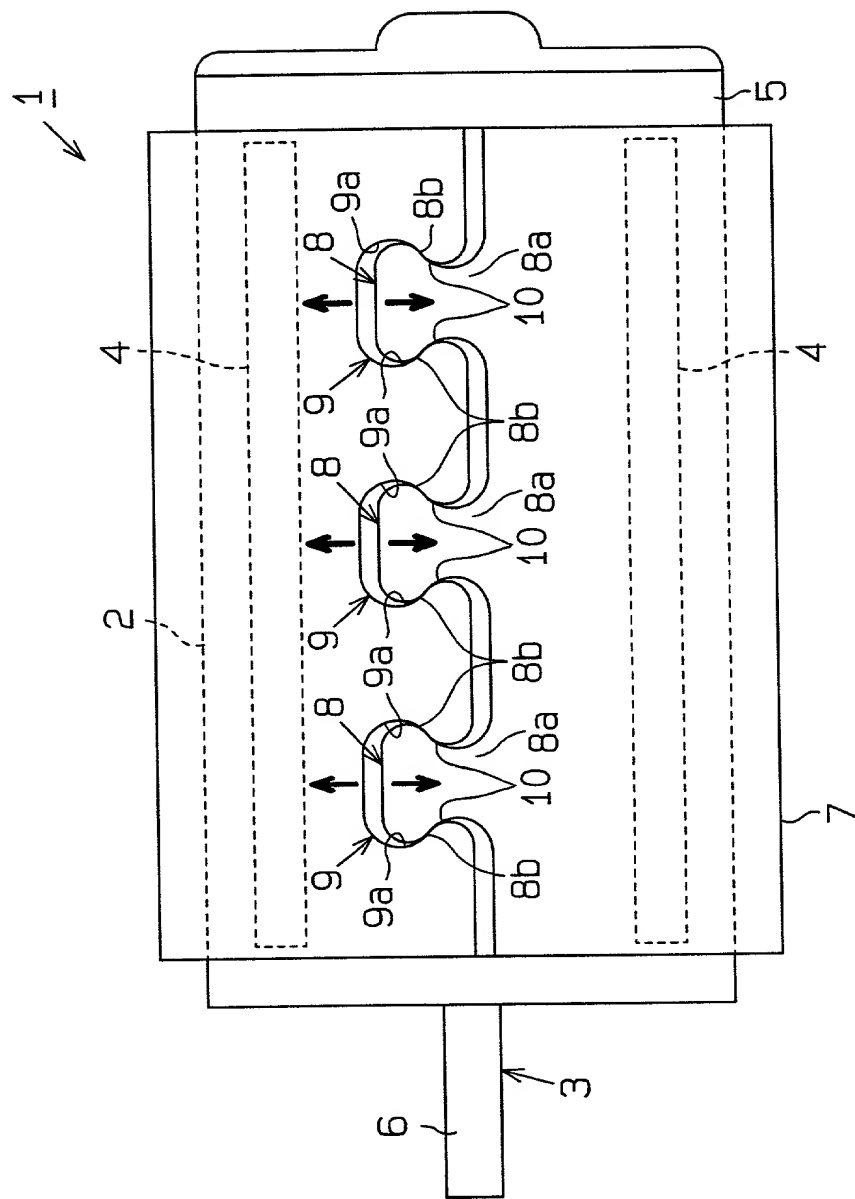


FIG. 2 is a schematic diagram of a device 100 in a first state.

FIG. 2

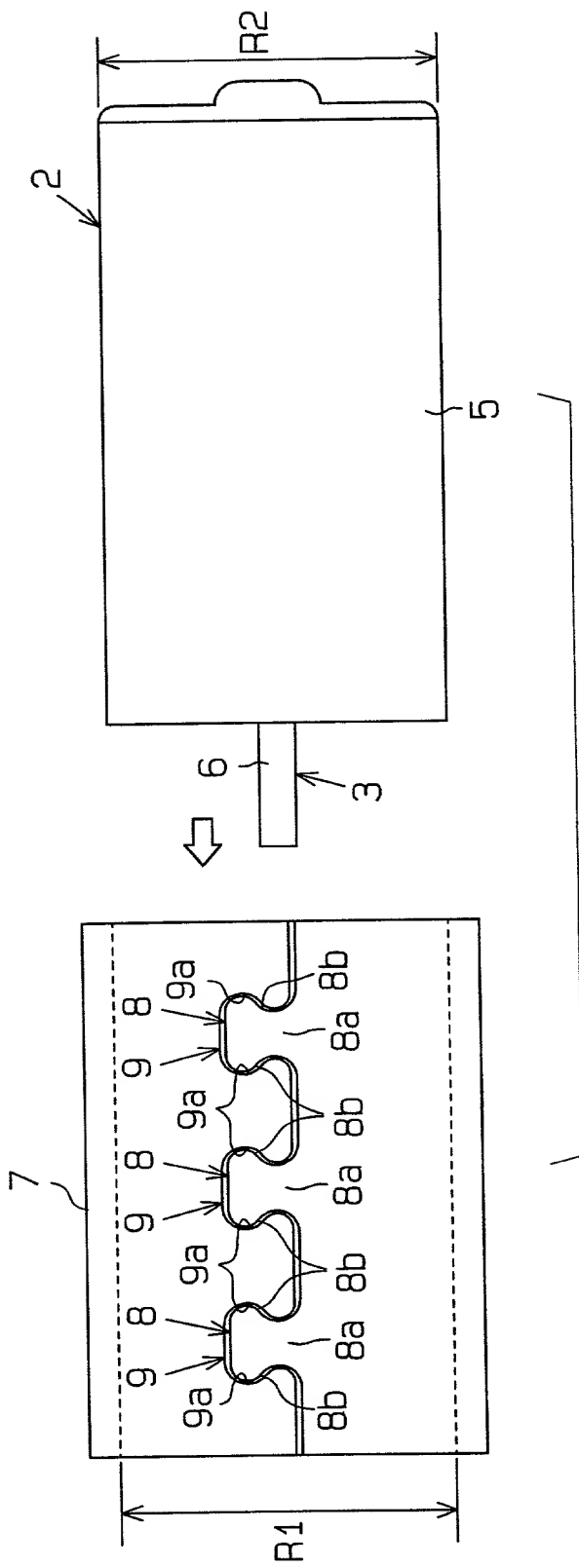


FIG. 3

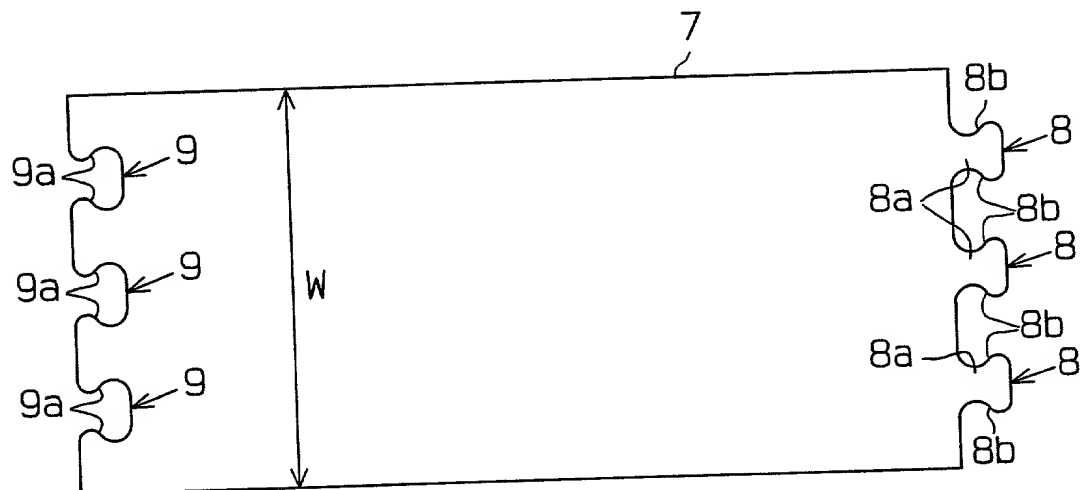


FIG. 4

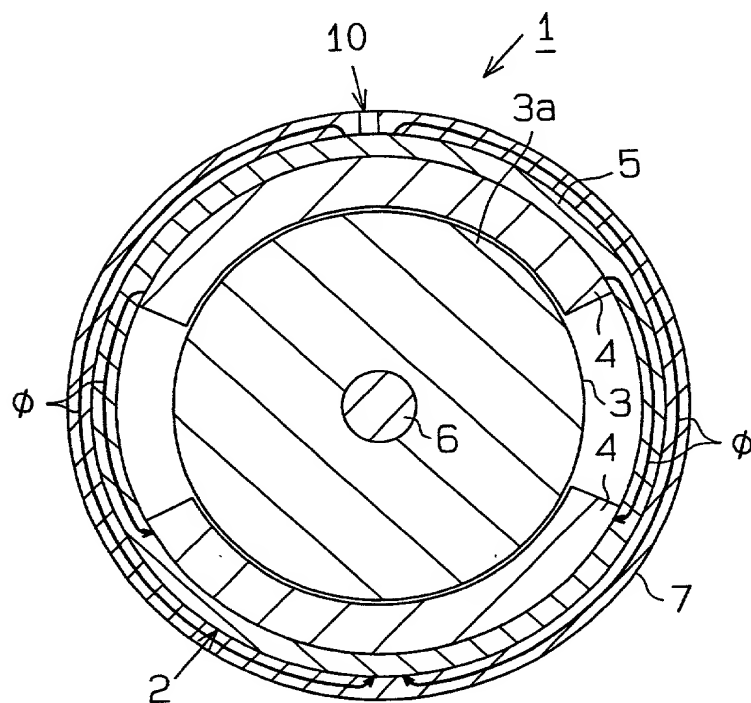


FIG. 5A

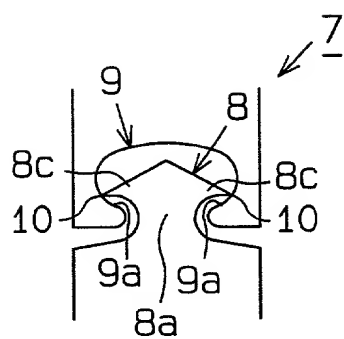


FIG. 5B

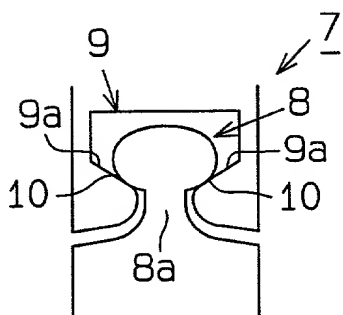


FIG. 5C

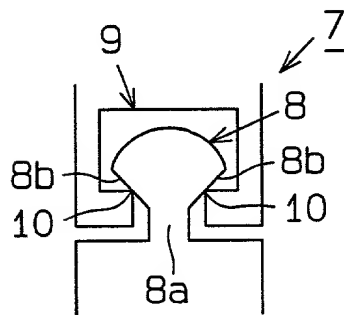


FIG. 6

PRIOR ART

